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INTERNET INFORMATION RETRIEVAL, PARALLEL SORTING, AND RANK-ORDER FILTERING BASED ON DYNAMICAL NEURAL CIRCUITS OF MAXIMAL VALUE SIGNAL IDENTIFICATION AMONG DISCRETE-TIME SIGNALS

ВИДОБУВАННЯ ІНФОРМАЦІЇ З ІНТЕРНЕТ, ПАРАЛЕЛЬНЕ СОРТУВАННЯ ТА ФІЛЬТРУВАННЯ РАНГУ НА ОСНОВІ ДИНАМІЧНИХ НЕЙРОННИХ СХЕМ ІДЕНТИФІКАЦІЇ МАКСИМАЛЬНИХ ЗА ЗНАЧЕННЯМИ СЕРЕД ДИСКРЕТИЗОВАНИХ СИГНАЛІВ

The design of mathematical models and corresponding functional block-diagrams of discrete-time neural networks for Internet information retrieval, parallel sorting, and rank-order filtering is proposed. The networks are based on the discrete-time dynamical K-winners-take-all (KWTA) neural circuits which can identify the K largest from N input signals, where $1 \le K < N$ is a positive integer. Implementation prospects of the networks in an up-to date digital hardware are outlined. In contrast to other comparable analogs, the networks are expected to combine such properties as high precision, speed and reliability of signal processing, low computational and hardware implementation complexity.

Keywords: mathematical model, functional block-diagram, Internet information retrieval, parallel sorting, rank-order filtering, discrete-time dynamical K-winners-take-all neural circuit, hardware implementation, signal processing, computational complexity.

Запропоновано проект математичних моделей і відповідних функціональних блок-схем нейронних мереж видобування інформації з Інтернет, паралельного сортування і фільтрування рангу, призначених для обробки дискретизованих сигналів. Мережі конструюються на основі динамічних нейронних схем типу "K-winners-take-all" (KWTA-схем), призначених для обробки дискретизованих сигналів, які здатні ідентифікувати K найбільших серед N вхідних сигналів, де $1 \le K < N$ – позитивне ціле число. Окреслено перспективу реалізації мереж у сучасному цифровому апаратному забезпеченні і їх можливі застосування. Очікується, що на відміну від інших близьких аналогів, мережі будуть поєднувати такі властивості, як високі точність, швидкість і надійність обробки сигналів, а також незначні обчислювальну складність та складність схемотехнічної реалізації.

Ключові слова: математична модель, функціональна блок-схема, видобування інформації в Інтернет, паралельне сортування, фільтрування рангу, динамічна нейронна схема типу "K-winners-take-all", призначена для обробки дискретизованих сигналів, схемо-технічна реалізація, обробка сигналів, обчислювальна складність.

1. Introduction

1.1. K-winners-take-all neural networks

Neural circuits of maximal value signal identification among discrete-time signals, in other words, K-winners-take-all (KWTA) neural networks are known to select K largest out of a set of N inputs, where $1 \le K < N$ is a positive integer [1] – [4]. In the special case when K is equal to unity, the KWTA network is the winner-takes-all (WTA) one, that chooses the maximal among N inputs [5] – [7].

1.2. Internet Information Retrieval

It is known that in the Internet information retrieval, the weights of N pages can be calculated using PageRank algorithm. Then, the PageRank results are displayed using, for instance, Quicksort algorithm. However, in the Internet information retrieval, instead of sorting all the results, usually only the ten or twenty most important ones with largest weights should be found within numerous results [8], [9]. Such a problem can be formulated as choosing the K most important within N results, where $1 \le K < N$ is a positive integer. Therefore the analogue KWTA neural circuit of low computational complexity was applied to solve this problem in [4].

1.3. Parallel Sorting

Sorting is considered as a fundamental operation of data processing [10]. In the case of parallel sorting, a sorting order can be represented as a permutation matrix. In such a matrix, "1" in the row labeled with a_i and column marked with c_j can be defined as the i-th item in an unsorted list and j-th item in a sorted list [8], [11]. In the case i=1,2,3,4,5, the corresponding permutation matrix

$$\begin{array}{cccccc} c_1 & c_2 & c_3 & c_4 & c_5 & \text{rank} \\ a_1 & 0 & 0 & 1 & 0 & 0 & 3 \\ a_2 & 1 & 0 & 0 & 0 & 0 & 1 \\ a_3 & 0 & 0 & 0 & 1 & 0 & 4 \\ a_4 & 0 & 1 & 0 & 0 & 0 & 2 \\ a_5 & 0 & 0 & 0 & 0 & 1 & 5 \end{array} \qquad (1)$$

represents an unsorted list $\{a_1, a_2, a_3, a_4, a_5\}$ and its ordered list $\{a_2, a_4, a_1, a_3, a_5\}$. The permutation matrix (1) can be transformed to the sorting matrix

$$\begin{array}{cccccc} S^1 & S^2 & S^3 & S^4 & S^5 & \text{rank} \\ a_1 & 0 & 0 & 1 & 1 & 1 & 3 \\ a_2 & 1 & 1 & 1 & 1 & 1 & 1 \\ a_3 & 0 & 0 & 0 & 1 & 1 & 4 \\ a_4 & 0 & 1 & 1 & 1 & 1 & 2 \\ a_5 & 0 & 0 & 0 & 0 & 1 & 5. \end{array} \qquad (2)$$

The sorting results in general case can be presented by

$$c_1 = S^1,\ c_{k+1} = S^{k+1} - S^k,\ k = 1, \ldots, N\text{-}1, \qquad (3)$$

where the elements of j-th column $S^j = \left[S_1^j, S_2^j, ..., S_N^j\right]^T$, j=1,2,3,…,N of the sorting matrix are determined by step functions of the analogue KWTA neural circuit from [3]. If N−1 state equations of the circuit are used and each equation computes one column of the sorting matrix from left to right with K increasing from 1 to N−1, then the only N−1 analogue KWTA neural circuits are necessary with a substantial reduction of the network complexity compared with the other analogue sorting networks with N^2 neurons [12].

1.4. Rank-Order Filtering

Rank-order filters (ROFs) are known to be nonlinear filters that identify, in time or spatial domain, the signal of k-th rank among all elements of an n-dimensional signal vector. Numerous methods have been proposed to design ROFs [8]. The output signals of the ROF can be given by

$$c = a^T\left(S_k^K - S_k^{K-1}\right), \qquad (4)$$

where S_k^K, k=1,2,…,N is a step function of the analogue KWTA neural circuit determined for K winners, S_k^{K-1} is a step function of the circuit obtained for K-1 winners, $\mathbf{c} = \left(c_{n_1}, c_{n_2}, ..., c_{n_N}\right)^T$ is an output signal vector of the ROF. However, the filtered signal demonstrates parasitic oscillations in the time points where corresponding input signal becomes equal to some other input signal. In order to remove these oscillations, the expression (4) was generalized on the case of processing such time-varying input signals which can be equal to one another in some time points. For this purpose the expression (4) can be extended to the following form:

$$c = a^T\left(S^K - S^{K-1}\right), \text{ if } R^K = 0, R^{K-1} = 0;$$
$$dc/dt = 0,\ c_0 = 0, \text{ otherwise,} \qquad (5)$$

where R^K is a residual function of the analogue KWTA neural circuit obtained for K winners, R^{K-1} is a residual function of the circuit determined for K-1 winners, $c_0 = 0$ is an initial condition. In the transient mode, output signals of the ROF are described by the degenerative differential equation of the system (5). In the KWTA steady state mode, the system (5) is reduced to the expression (4) which is a particular case of (5). It was shown that using (5) instead of (4) leads to completely removing parasitic oscillations on the ROF outputs in the time points of equal input signals.

2. The problem statement

Let us assume that neural networks which are based on the neural circuits of maximal value discrete-time signal identification are used for Internet information retrieval, parallel sorting, and rank-order filtering. It is necessary to show that as a result, solutions which are more precise from computational point of view, more faster and reliable comparatively to these derived by other analogous methods can be obtained when requirements to a network size and power are not very high. It should be shown that the network of Internet information retrieval designed in such a way may have low computational complexity, obtained parallel sorting network can be simple from a hardware implementation complexity point of view, and derived rank-order filter network may be suitable for correct, without parasitic oscillations output signal processing which have equal values in some time points. It is also necessary to outline a hardware implementation perspectives of the networks in an up-to-date digital hardware.

3. Principles of designing discrete-time neural networks of Internet information retrieval, parallel sorting, and rank-order filtering

3.1. Deriving of mathematical models of the networks

As it can be seen from the Section 1, a basic unit of the networks of Internet information retrieval, parallel sorting, and rank-order filtering is the analogue KWTA neural circuit. However, it is known that discrete-time neural networks comparatively to continuous-time analogs demonstrate a more high precision of signal processing, they are more reliable, more suitable to implement in software, and can be implemented in an up-to-date digital hardware for real time signal processing [13]. In [14], mathematical model and corresponding functional block-diagram of discrete-time KWTA neural circuit built in one-layer competitive architecture performing the dynamic shifting of input signals to obtain K winners was proposed. The circuit is globally stable and convergent to KWTA operation in finite number of iterations. The results of comparison show that the circuit achieves higher speed of signal processing than other close analogs. The computational and hardware implementation complexity of the circuit is close to that of simplest KWTA networks. The circuit can process any finite value distinct signals. Periodical resetting and corresponding supervisory circuit for repetitive signal processing are not necessary.

In this paper, the mathematical model of the discrete-time KWTA neural circuit [14] is suggested to simplify and use for Internet information retrieval, parallel sorting, and rank-order filtering. In particular, the discrete-time residual function and signum (hard limiting) function of this circuit can be replaced with the discrete-time counterparts of the simplified continuous-time residual function and step function.

Obtained in such a way, the simplified mathematical model of the discrete-time KWTA neural circuit can be directly used for Internet information retrieval. The derived model will be of O(N) computational complexity. Since other comparable analogs for Internet information retrieval which use Quicksort algorithm have O(NlogN) computational complexity on average therefore the obtained model will need less computational time than these competitors [8], [9].

The obtained simplified mathematical model of the discrete-time KWTA neural circuit can be also used for parallel sorting. In this case, discrete-time step functions may be used for determining the elements of j-th column $S^j = \left[S_1^j, S_2^j, ..., S_N^j\right]^T$, j=1,2,3,…,N of the sorting matrix of the sorting results (3).

The mathematical model of the discrete-time ROF neural network is proposed to derive on the base of the system of algebra-differential equations (5) which contains the simplified residual function and step functions. In particular, in the transient mode, output signals of the ROF will be described by the degenerative discrete-time equation corresponding to the degenerative differential equation of the system (5). In the KWTA steady state mode, the mathematical model of the ROF will be reduced to expression (4).

3.2. Designing functional block-diagrams of the networks

As it can be seen from the functional block-diagram of the discrete-time KWTA neural circuit [14], discrete-time counterparts of the simplified continuous-time residual function and step function [4], and from (3) – (6), the functional block-diagrams of the designed neural networks for Internet information retrieval, parallel sorting, and rank-order filtering will contain the blocks of discrete-time summation, multiplication, integration, step function, external sources of constant and controlled signals. Therefore, such networks can be implemented in an up-to-date digital hardware using such traditional digital components as adders, hard-limiting quantizers (switches), digital integrators, and external sources of voltage or current.

The discrete-time neural network which is proposed to design for parallel sorting is expected to be more simple from hardware implementation point of view than other comparable sorting networks with N^2 neurons since the only N−1 basic discrete-time KWTA neural circuits are necessary with a substantial reduction of the network complexity for processing N inputs. In particular, the 1WTA discrete-time neural circuit can be used to identify the largest element of the list of inputs. Next, the 2WTA circuit selects the second item in the list without recounting the first item. As such, the whole list of N items can be sorted by using the (N−1)WTA discrete-time circuits without the need to choose the last item.

A resolution ability of the designed neural networks is infinite theoretically, i.e. if input signals are distinct, then such the networks can always process them correctly. Note that the ROF neural network is capable to process correctly also time-varying input signals which can be equal to one another in some time points. Practical resolution of the networks will be limited by precision of the network hardware implementation.

Since an operation of the basic discrete-time KWTA neural circuits is independent on initial values of its state variables, a functioning of the designed networks be independent on initial conditions which can accept arbitrary values in a given range. Therefore the networks will not require periodical resetting for repetitive signal processing, additional supervisory circuits for resetting, and spend additional processing time on this operation. This allows to simplify the hardware and increase a speed of signal processing that is important for real time operating of designed networks.

3.3. Perspectives of hardware implementation of the networks

The implementation of the designed neural networks for Internet information retrieval, parallel sorting and ROFs will be simulated using software. Such simulations should confirm theoretical results obtained in the project. However, the processing speed in this case may be not fast, especially to meet the demands of real time. Therefore, microprocessors and digital signal processing can be not suitable for parallel designs of such networks. For real time applications, the designed networks can be implemented in an up-to-date digital hardware. Comparing with the analogue implementation, as known, a digital hardware

is more computationally precise and reliable as long as the requirements for the size and power efficiency are not high. The digital implementation of the designed networks is expected to have a better repeatability, lower noise sensitivity, better testability, higher flexibility, as well as compatibility with other types of preprocessors [13].

It is known that for modern digital neural network hardware FPGA-based implementations, ASIC-based implementations, and DSP-based implementations can be used. Since DSP-based implementation is sequential, it does not preserve the parallel architecture of the designed networks. ASIC implementation can be used for hardware realization of the networks, although it does not offer re-configurability by the user in order to improve the network performance. The FPGA implementation achieves a comparable accuracy with the traditional solutions based on general-purpose computers. An FPGA as an implementation hardware combines the reprogrammability advantage of general purpose processors with the parallel processing and speed advantages of customer hardware. The size and speed evaluation of FPGA reveals its low cost in terms of logic and memory [15]. To implement the networks in a hardware, the FPGA based reconfigurable computing architecture is quite suitable because the parallel structure of FPGA matches the topology of the designed networks and offers flexibility in reconfiguration. The architecture of the designed networks and training algorithms can be implemented on a FPGA chip performing an on-line training. Such computational characteristics of the networks as modularity and dynamic adaptation can also be realized in FPGA hardware. Using FPGA, the proposed networks can be implemented through parallel computing in a real-time hand-tracking systems [16]. Due to the relatively high capacity, high density, short design cycle, and short time to market when using EDA tools, FPGA can be considered as the most applicable microelectronic technology for the designed networks.

4. Conclusions

The proposed principles of designing artificial neural networks are important for improving of problem solving of Internet information retrieval, parallel sorting and rank-order filtering, making better corresponding software and digital hardware, and also for different applications. Moreover, described approaches can be applied for increasing of effectiveness other neural networks and dynamical systems. Presented designing tolls of the networks can be used in different areas, in particular, for improving image processing, signal processing, speech processing, noise removal, in computerized tomography, for biomedical imaging, pattern recognition, coding, in digital TV, etc. [17] – [20].

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HIGH-FIELD STRENGTH THE SOURCES BASED ON TILTED PULSE FRONT PUMPING: OPERATION PRINCIPLE AND PERSPECTIVES

ВИСОКОАМПЛІТУДНІ ТЕРАГЕРЦОВІ ДЖЕРЕЛА З ПОМПУВАННЯМ НАХИЛЕНИМ ФРОНТОМ: ПРИНЦИП РОБОТИ І ПЕРСПЕКТИВИ

The terahertz wave generation using tilted pulse front pumping (TPFP) is the most advanced technique nowadays. In this paper we made a brief review of common terahertz sources. Theoretical aspects and experimental results of tilted pulse front pumping on $LiNbO_3$ have been discussed.

Key words: TPFP, $LiNbO_3$, Terahertz wave, optical rectification.

Генерація електромагнітних хвиль терагерцового діапазону з використанням методики помпування нахиленим фронтом є найсучаснішим підходом на сьогодні. У статті зроблено огляд традиційних джерел терагерцового випромінювання. Також описано теоретичні аспекти й експериментальні результати генерації хвиль за допомогою накачки з нахиленим фронтом на кристалі $LiNbO_3$.

Ключові слова: помпування нахиленим фронтом, $LiNbO_3$, Терагерцові хвилі, оптичне випрямлення.

Problem statement

The development of new terahertz sources is an extremely topical nowadays due to rapid development of new materials and nanostructures. Terahertz band of electromagnetic wave spectrum, which is typically governs frequency region from 0.3 THz up to 20 THz [1], has a lot of applications: material characterization, security systems, medical applications etc.