Comparative analysis of characteristics of special-purpose versus reconfigurable hardware accelerators

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Abstract – Present paper deals with a review of specific features of special-purpose and reconfigurable hardware accelerators, the criteria of their comparison have been specified, and a comparative analysis of the characteristics according to the above criteria has been carried out.

Key words – computer systems, hardware accelerator, FPGA, processor, high-performance systems, reconfigurable accelerators.

I. Introduction

Traditionally, complex computational tasks are being solved using high-performance computing systems including, in particular, multi-processor computer systems that use the computation process paralleling approach [1]. However, real performance of multi-processor computer systems oriented to the conventional methods of organization of parallel computations and based on the serial microprocessors often does not exceed 10–15% of their peak performance. The reason is the necessity of realization of the inter-processor exchange procedures and synchronization of serial processes executed in the system processors. Alternatively, one may use the hardware computation accelerators that accelerate execution of specified algorithm or a class of algorithms.

The hardware accelerator is a device that executes a limited set of functions to increase the performance of computer system or its separate parts [1]. It is designed to execute on the hardware level the complex algorithms of processing large data arrays that requires much time and resources for software execution at the general-purpose computer. Usually, when using the hardware accelerator, the time spent for solving the tasks is substantially reduced as compared to that using the general-purpose computer allowing, thus, a great number of data to be processed rapidly. This is achieved due to a total paralleling of the hardware execution of algorithm using the special-purpose integrated circuit (e.g. 3D-Accelerator, i.e. that for the video image processing, where it is necessary to carry out a number of complex computations to create a 3-D image, paint a texture and dynamics of object motion) [1].

There are two basic approaches to realize the hardware accelerators. The first is related to the creation of the special-purpose hardware accelerators, i.e. those comprising a special-purpose processor on the basis of a full-custom integrated circuit. Such approach provides the highest accelerator performance, however, due to high cost of full-custom integrated circuit production, it is reasonable in case of mass production only, and this is often inexpedient in view of a narrow functional orientation. The second approach means the use an FPGA (Field Programmed Gate Array) chip, that is the matrix of programmed logic cells with universal structure, as the basis of a special-purpose processor. The programmable logic cells of FPGA allow one to create a special-purpose processor integrated circuit by using required logic elements and organizing communication between them. Due to the basic flexibility of logic cells, the FPGA-based special-purpose processors (in other words, those synthesized in FPGA) have lower performance as compared to the full-custom very large scale integrated circuits but allow the total paralleling of algorithm execution to be achieved.

II. Specific features of special-purpose hardware accelerators

The most widely used special-purpose hardware accelerators (SPHA) are as follows:

- CELL processors [2, 3] co-developed by the IBM, Toshiba and Sony;
- circuit boards developed by the ClearSpeed [4, 5] (UK – USA);
- GPGPU units and circuit boards [6–7] developed by the ATI and Nvidia;
- GRAPE circuit boards [8, 9] co-developed by researchers from the Tokyo University and Japan National Astronomical Observatory.

In average, transferring computations from the general-purpose processor to the accelerator ensures in many tasks the 5–30 times acceleration, while in some cases this value is even higher.

Figure 1 shows the generalized structure of the CELL processor [10] that is the basis of the relevant hardware accelerators on the level of its processing elements, memory and communication equipment. Other SPHA processors [10] have, in general, the similar structure.

According to the results of analysis of the SPHA architecture and technical data [10], one may trace the general trends of their development: i) increasing number of parallel processing elements and memory space; ii) increasing operating frequency of processing elements and memory blocks; iii) increasing memory bandwidth due to increasing number and capacity of data exchange channels; iv) involvement of new special-purpose computing modules into SPHA for fast execution of mathematical operations; v) modification of mechanisms of parallel use of the SPHA resources by a number of computing processes of the host computer.

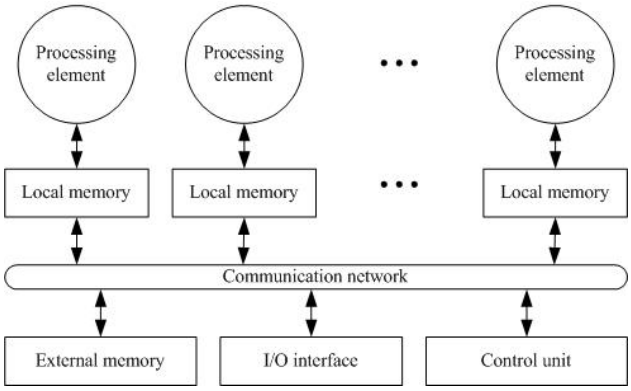

Fig. 1. Generalized structure of the CELL processor

It should be noted that such trends in development are today inherent in the general-purpose programmable processors as well being evidenced by: i) transition to multi-coring and increase of the cores number; ii) multithreading on the computing core level; iii) expansion of the command system and introduction of new functional modules into the arithmetic and logic devices. Thus, the general-purpose processors and SPHA demonstrate a tendency of convergence, and one may expect that this tendency will be kept in future as well.

III. Specific features of reconfigured hardware accelerators

An approach of creating the general-purpose high-performance systems on the basis of the general-purpose microprocessors and special-purpose processors allows high indices of system performance to be obtained for solving tasks based on the algorithms that the special-purpose processor is oriented to. At the same time, it is necessary to provide flexibility and required performance of performing an arbitrary computational task.

A question arises: how one can combine the general-purpose processors and hardware orientation to the algorithms under execution? The answer is the use of an approach to construct the high-performance computing systems applying the reconfigurable components that is an alternative to those considered above.

The possibility of changing the FPGA configuration (i.e. changing the algorithm executed by FPGA by weaving in FPGA the model of other special-purpose processor) had made a basis for an approach of creating the hardware accelerators named the reconfigurable ones. The hardware accelerator reconfigurability means its capability to change configuration (i.e. to arrange the internal structure of functional units and their relationships) to provide optimal mapping of specific features of executed algorithms on the hardware level in order to achieve the maximal performance of their execution.

A generalized FPGA structure is shown in Fig. 2 [11]. The following abbreviations are used to denote the relevant units: PCM (Programmable Switch Module) and CLB (Configurable Logic Block).

The use of FPGA as the basic elements for creating the hardware accelerators allows one to:

- Set the hardware accelerator for executing a particular algorithm not on the production stage, but after that by synthesizing the required special-purpose processor in FPGA.
- Reset the hardware accelerator for executing another algorithm by synthesizing another special-purpose processor in FPGA.
- Build high-performance computing systems on the basis of the general-purpose microprocessors and reconfigurable accelerators and obtain high performance indices of such systems when executing arbitrary tasks, since the arbitrary special-purpose processor could be realized in the reconfigurable accelerator.

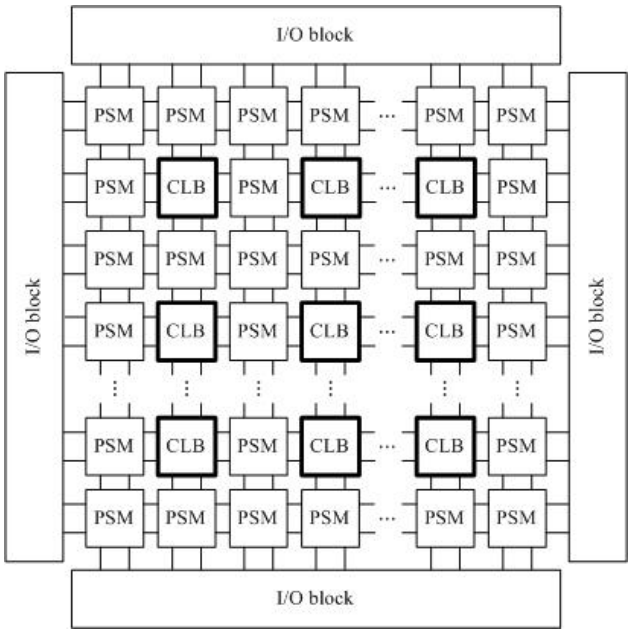

Fig. 2. Generalized structure of the FPGA

The reconfigurable accelerators Advance X620 and e620 Accelerator Boards [12] produced by the ClearSpeed, H100 Series [13] (NALLATECH), COPACOBANA [14] (SciEngines), RPU100 (DRC) [15], RCHTX (Celoxica) [16] and others are now being used on the market most widely.

Since that approach to constructing accelerators does not include the use of the full-custom integrates cirquits, the cost of the hardware accelerator depends mainly on that of the FPGA chip. Furthermore, since FPGA are not being initially related to a particular computation algorithm, the possibilities of using such hardware accelerators are limited by the FPGA functional and capacitance characteristics. The accelerator circuit boards may be completed with several FPGA chips to ensure achieving the necessary computational capacities. Otherwise, these should by the multi-board multi-block units [14].

IV. Comparison of characteristics of the special-purpose and reconfigurable hardware accelerators

Based on the analysis of the architecture of the special-purpose accelerators processors [10] and the principles of constructing the reconfigurable accelerators [17], one may distinguish their common features and make a comparison (see Table 1).

As seen from Table 1, the FPGA-based accelerators possess principal advantages over the special-purpose accelerator processors, namely:

1. The way of executing the computational algorithms does not include command fetching and decoding, operand fetching and storing results (each of this actions requires referencing to memory), and this allows much higher performance to be achieved (i.e. transferring computations from the available high-performance general-purpose processor to the special-purpose accelerator ensures in many tasks acceleration by 5–30 times, while that in FPGA reaches 1–3 orders of magnitude).
2. The availability of the means of automatic creation of the program models of the special-purpose processors as well as the presence of means of their logic synthesis in FPGA simplify execution of computational algorithms as compared to the special-purpose ones.

Moreover, FPGA are characterized by much less power consumption as compared to the special-purpose accelerators.

TABLE 1

COMPARISON OF THE SPECIAL-PURPOSE HARDWARE ACCELERATORS WITH RECONFIGURABLE ONES

Special-purpose accelerator processors	FPGA
The set of the processing elements each of which is capable of executing a specified set of operations, interfaced with the local or common memory is the **basis of the special-purpose accelerator.**	The set of the configured logic cells each of which is capable of executing a specified set of data processing operations and their storage, as well as the intercommunication lines is the **FPGA basis.**
The type of operation executed by a certain processing element is set by the program and is changed in time of executing the computational algorithm with the program command change.	**The type of operation executed by a certain configured logic cell** is set by the FPGA configuration and is stable in time of executing the computational algorithm.
Transition in time from one operation of the algorithm executed by the special-purpose accelerator to another one is made by changing the program command. This, besides the direct execution of operation (as it is done in FPGA), also means command sampling and decoding, operand sampling and results storing. In this case the communicative environment and the memory are used.	**Transition in time from one operation of the algorithm executed by the special-purpose processor implemented in FPGA to another one** is made by transferring the data from one configurable logic cell to another one via the relevant communication lines determined by the FPGA configuration.
The parallel information processing in the special-purpose accelerator is realized in a program way by mapping the parallel branches of executed algorithm into the set of parallel subprograms adapted to the structure of the special-purpose accelerator processor as well as their parallel execution. In this case the above mapping is done by the programmer who is aware of programming technique for the relevant processor (e.g., CUDA for the graphical processors of the Nvidia). Up to date, the methods of automatic creation of special-purpose accelerator-related programs of those written for conventional single-processor computer systems using procedure programming languages are not available.	**The parallel information processing in FPGA is realized** in the hardware way by mapping the parallel branches of executed algorithm into the set of its logic cells and setting the relationships between them. In this case the above mapping is done automatically by means of the relevant program means (e.g., ISE from the Xilinx company and Quartus II from the Altera company) of program models of special-purpose processors presented using the hardware means description. Up to date, the methods of automatic creation of special-purpose processors for conventional single-processor computer systems using procedure programming languages, in particular, ANSI are available.

Conclusion

A comparative analysis of the special-purpose hardware accelerators and FPGAs has been carried out with respect to the way of implementing in there the computational algorithms. This analysis has shown that FPGA have a series of principal advantages over the special-purpose accelerator processors. This proves the promising character of creating the high-performance computer systems on the basis of the general-purpose processors and reconfigurable logic as well as their higher potential abilities, first and foremost, related to the "performance to power consumption" ratio as compared to the available up to date system based on the general-purpose processors and special-purpose accelerators. This indicates the expediency of developing such conceptual approaches to organizing their functioning and architectural solutions that will allow the property of reconfigurability to be used and information processing to be simplified.

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